

# TECHNICALLY speaking

BY G. CARRASCO, DR. J. HARRIS, T. BECKETT, AND E. RUBEL, CMC LABORATORIES, TEMPE, ARIZ.

## New Technology for Electroplating Metal Layers Aims to Improve Thickness Control

CMC Laboratories has developed a new technology for electroplating metal layers that results in significant improvements in thickness control.<sup>1</sup> CMC's technology, which is called "Smart Rack," utilizes active control of the plating process to improve thickness versus traditional passive controls such as current thieves. CMC's Smart Rack technology entails a new electroplating circuit as well as a completely different approach to rack design. Though this technology was developed for electronic devices or package applications, it can easily be applied in other areas that utilize precious metal plating.

The focus of this new technology is to narrow the distribution of plated layer thicknesses across a plating rack. Narrowing this distribution can have a significant impact on precious metal plated layers, such as Au, Pt, Pd, Rh, and Ir. When a minimum thickness of these expensive metals is specified, as is typical, a narrower distribution results in less metal used for significant cost savings.

A tighter plating distribution can also be important for other metal plating processes. For example, currently most wafer bump plating is done using low throughput, high tool cost fountain platers. For small wafer size (< 6 inches), it may be possible to use Smart Rack technology to bump multiple wafers at one time in a rack configuration. Since Smart Rack only improves part to part thickness control, not the thickness distribution across a part, the technology would not help for very large wafers.

The ability to plate AuSn at the eutectic composition on die attach pads would also be very important in many high power electronic applications. However, since the composition of AuSn varies with current density, it is very

difficult to achieve the 80/20 eutectic across a large plating rack. AuSn compositions that are off eutectic will not melt at the 400C process temperature.<sup>2</sup>

Traditional electrolytic plating uses a plating rack that is made of a highly conductive metal such as copper or stainless steel. All of the parts being plated are attached to this rack. During the plating process, the rack is attached to a constant current power supply (plating rectifier). Current is pumped through the rack structure, forcing the plating reaction to occur at the interface between the conducting work parts and the plating solution or electrolyte.

The plating rate at each individual part depends on a number of factors:

- The electrical current density at the individual part
- The availability of metal ions in solution at the location of the individual part
- The availability of other electrochemical reactants at the plating interface which compete with the plating reaction

Macroscopic factors that affect these more microscopic reactions include:

- Density of plating parts surrounding the individual, part being plated
- Resistance drops across the plating rack
- Location of the part on the rack
- Plating rate
- Uniformity of the electrochemical environment including variations in solution chemistry, temperature, agitation

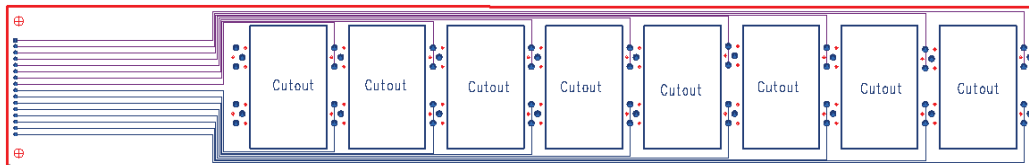


Figure 1a. Electrically isolated rack pieces.

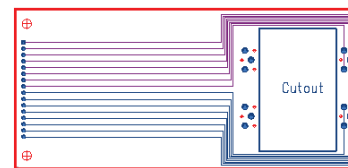


Figure 1b

All of these variations lead to thickness variation in parts from one location of a plating rack to the next.

## TECHNICALLY speaking



Figure 2. Smart Rack for PCBs.

Typically the thickest parts are located along the edge of the rack and the thinnest parts are located near the center. One reason for this trend is that the flow of metal ions to be plated is unimpeded near the edge of the rack, but near the center of the rack, surrounding parts “screen” the metal ion flow from their neighboring parts. This competition for plating ions results in a thinner deposited layer and a lower plating current density.

### DESCRIPTION OF SMART RACK CONCEPT

The essential feature of the Smart Rack concept is to individually control the electrical current that flows to each piece during the plating process. This individual current control allows active and direct control of the plating process, which can very significantly narrow the plating thickness distribution. This direct method is much more effective than indirect methods such as current thieves, and the range of adjustment is considerably higher. For example, if desired, the programmed current density of two parts on the same rack could vary by factors of 2 or more. In addition, this method is much easier to implement and control because changes in current densities can be effected by adjusting inputs to the plating program rather than making any physical changes to the plating bath or set up.

To accomplish this requires two significant changes compared to the traditional plating approach. First, the plating rack must be constructed so that individual electrical current conductors are connected to each individual piece on the rack, and thus each piece is electrically isolated from all of the other pieces. The rack, rather than being a large conductor, is now an insulator with individual wires or embedded metal traces, to each piece. This is shown in the diagram in Figure 1. In this Figure, you can see the cut out area where 2 parts are located and the traces to each part from the top contact array shows in the detail drawing.

One option for fabricating this type of rack is to utilize standard printed circuit board (PCB) technology which incorporates thick copper traces within a fiber reinforced epoxy insulator. This structure can then be coated to protect it from the aggressive plating chemicals. An example of a PCB technology Smart Rack is shown in Figure 2.

The second significant change is the presence of a new

circuit, which can control the current to each individual piece at a preprogrammed value. (There will be a more detailed description of this circuit later in this paper.) This circuit acts like an individual programmable current supply for each piece. However, due to the availability of miniature micro-controllers, the overall size of the control circuit can be made very small, and even mounted on the rack itself.

### SMART RACK PLATING RESULTS

#### Nickel Plating

The first set of results described here are for Ni plating from a traditional nickel sulfamate plating bath. Overall current density was 20 amps/sq. ft. with a bath temperature of 125°C. The pieces plated were copper substrates.

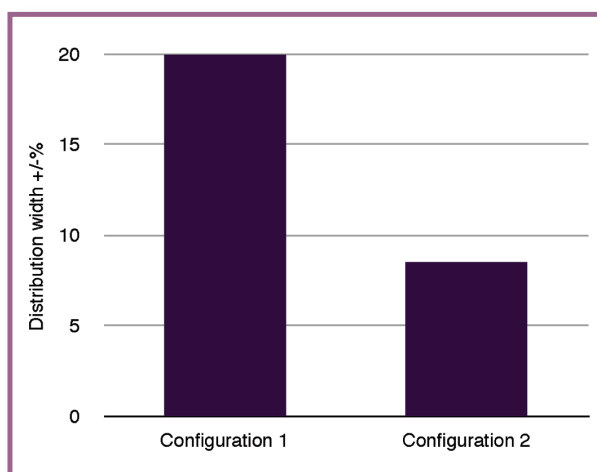


Figure 3. Comparison of plating thickness distribution in two scenarios.

The plating rack held 16 pieces and could be run in two different configurations. If all the plating locations were shorted together, the rack simulated a traditional plating rack. If each conductor was controlled individually, this represented the Smart Rack technology.

Figure 3 shows the width of the plating thickness distribution for two different situations. The first plating configuration has all of the parts shorted together and a constant current run through the entire rack. This configuration is the traditional plating bath set-up. Note that the total distribution width was +/- 20%, which is typical for a Ni bath.

In the second configuration, the individual traces to each part were isolated and a constant and equal current was run through each part. Said differently, the Smart Rack circuit forced the exact same current to flow through each part, irregardless of location on the plating rack. Note that, in this case, the distribution width dropped to +/- 8.5%, over a factor of 2 improved. This result demonstrates the dramatic reduction in the distribution width that can be accomplished by forcing the same current density through each individual piece during plating.

Because of the significant flexibility inherent in the

## TECHNICALLYspeaking

Smart Rack approach, further improvements can be made by individually adjusting the current density at each point to minimize the distribution width. To do this, small increases in current were programmed into parts with slightly lower than mean thickness, and small decreases in current were programmed into parts with higher than mean thickness. The result, shown as Configuration 3, had a distribution of +/- 3%. This is shown along with the previous results in Figure 4.

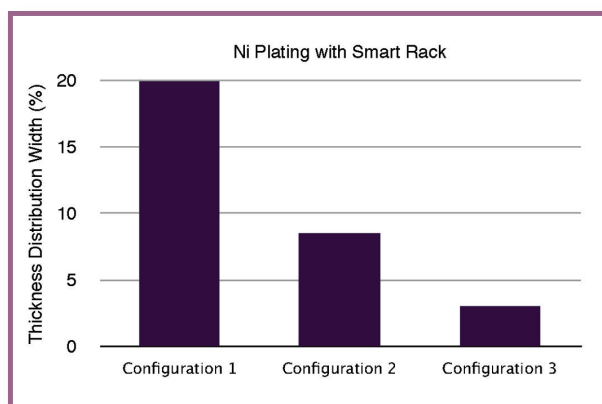


Figure 4.

### Silver Plating

Figure 5 below shows the results for Ag plating.

### DISCUSSION

The results above illustrate that individual current control can have a dramatic impact in reducing the thickness distribution during electroplating, even for materials like Ni that are typically very difficult to control.

Another interesting aspect of this technology is the

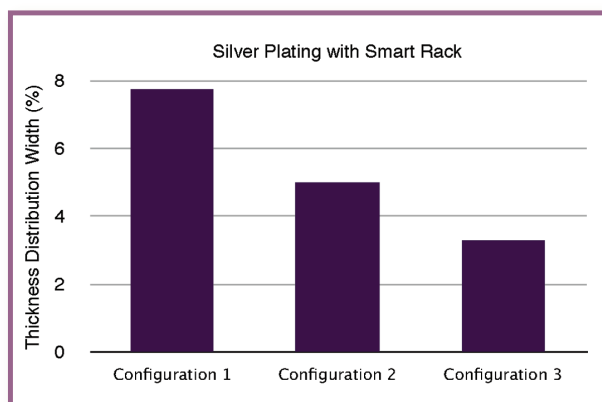


Figure 5

comparison between Configuration 2 and Configuration 3. At first pass, it would appear that setting a fixed and equal constant current at each plating site should yield the minimum distribution width.

Since a constant electrical current is flowing through

each part, the difference in plated layer thicknesses across the rack in Configuration 2 must be attributable to differences in plating versus non-plating electrochemical reactions at the part surface. By increasing the current density slightly for the lower thickness parts, as is done in Configuration 3, it is clear that the rate of plating reaction can be brought closer to plating rate for the mean thickness parts. Thus, differences in the plating reaction rates from one area on the rack to the next can be minimized by relative adjustments of current density as is shown for Configuration 3. This idea is illustrated schematically in Figure 6.

### DESCRIPTION OF THE SMART RACK CIRCUIT

There are three major portions of the control circuitry. A computer (which could also be a micro-controller), a master control circuit and an individual current control circuit for each part. The computer stores all of the programmed information, the Master Control Circuit (MCC) can measure the electrical current flowing in each individual Current Control Circuit (CCC) and send required adjustments to the CCC as needed.

The plating process utilizing the Smart Rack technology has two segments. Programming the control circuit followed by the plating segment.

The key steps in the program segment are:

1. Enter the base current density into the program
2. Enter the plating time
3. Enter the size of the plated surface on each part
4. Input any current density adjustments for each individual part from the base current level, as in Configuration 3 (if no changes are entered, the current density will be the same for all of the parts, as in Configuration 2).
5. Start the program, which initiates plating

Here is what the control circuitry does during the plating cycle:

1. Each individual part is controlled by its own constant current circuit (CCC). During the first phase of plating, the computer sends the desired individual current density value to each individual CCC.
2. Current begins to flow and plating starts
3. A master control circuit (MCC) reads the current value at the first part and compares it to the programmed value. The MCC then sends any required current adjustments to the CCC until the programmed current set point is met.
4. MCC scans to the next part and repeats the same process
5. After the last part is adjusted, the MCC returns to the first part and the cycle repeats.
6. This process continues until the plating cycle is completed.

# TECHNICALLY speaking

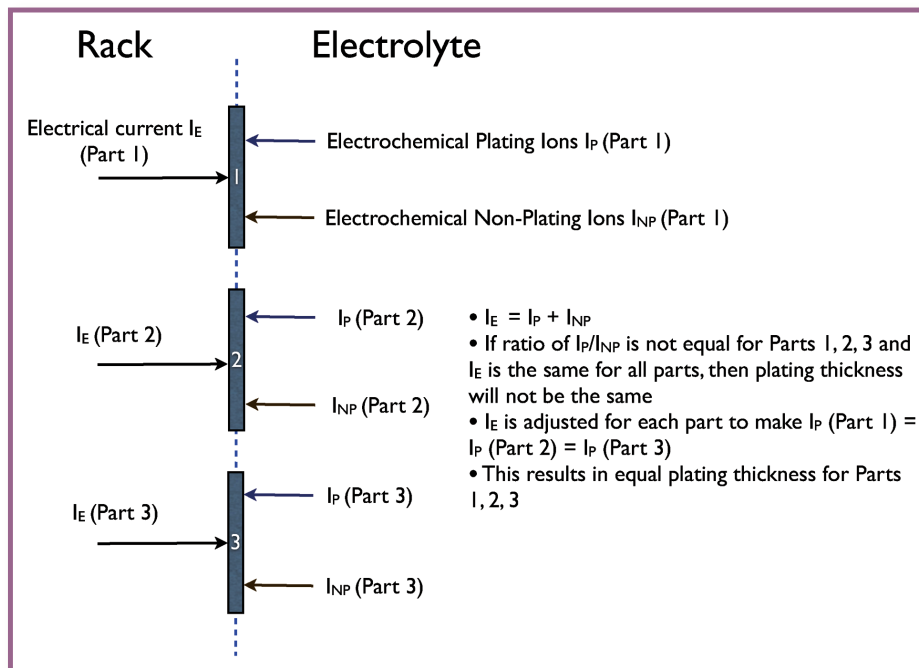


Figure 6. Variation in plating reaction rates from one area of the rack to another.

Thus, the purpose of the CCC is to act as a miniature constant current source for each individual part. The goal of the MCC is to monitor the CCC output and make any required adjustments to keep the output current at the required value (which is stored on the computer). It is clear that an individual CCC unit for each part is necessary in order to have maximum flexibility in adjusting the electrical current at each part. Furthermore, this flexibility is at the core of the Smart Rack technology's ability to dramatically narrow plating layer thickness distributions. (A schematic of the control circuit is shown in Figure 7.)

## APPLICATIONS FOR SMART RACK TECHNOLOGY

There are a number of applications where Smart Rack technology can have a strong impact in improving performance and manufacturability.

- **Noble metal plating to reduce the amount of material required to meet minimum thickness and, thus, lower cost.** Key metals would be Au, Pt, Pd and Rh.
- **Rack plating AuSn for solder or eutectic die attach.** For this application, Au and Sn layers are deposited on plated surfaces and then diffused. The deposited layer thicknesses must be very consistent (+/- 3%) in order to achieve eutectic composition melting.
- **Uniformity of thick plated layers such as Cu conductors.** Because the conductors can be very thick (50–500  $\mu\text{m}$ ), large variations in Cu thickness can lead to dimensional tolerance issues for the final plated part.
- **Bumping wafers that are 6 inches or less on a plating rack rather than using a fountain plater.** The advantage is higher throughput and lower tool cost.

## SUMMARY

This paper has described a new electroplating technology that is focussed around individual electrical control at each plating site. This electrical control is achieved by a special control circuit that monitors and adjusts the electrical current during plating at each site to a pre-set value. This approach also requires a plating rack that is made from an electrically insulating material with metal traces to each plating site. This type of rack can be made using PCB fabrication technology to lower cost and weight.

If electrical current is set to the same value at each plating site, a significant improvement in the plating thickness distribution can be

achieved. However, if small additional adjustments are made that boost the thickness in areas below the mean value, and reduce the thickness in areas above the mean value, even a narrower distribution can be attained. The basic electrochemistry behind this observed phenomena was discussed.

Data was presented for Ni plating and Ag plating. For Ni, the distribution using a traditional "shorted" rack, where all of the parts are connected to each other and to the cathode, had a distribution of +/- 20%, which is typical for Ni sulfamate. If all parts were run at an individually controlled and equal value, the distribution width dropped to +/- 8.5%. If each plating location current was optimized, as discussed above, the distribution width dropped to +/- 3%. For silver, the results were similar. The shorted rack had a distribution of +/- 7.8%. The constant current rack dropped the distribution width to +/- 5% and the individually controlled rack had a distribution width of +/- 3.3%.

## REFERENCES

1. Submitted to U.S. Patent Office 1
2. Semiconductor International, Oct. 1, 2007

## ABOUT THE AUTHORS

**Thomas Beckett** is a metal finishing specialist and plating consultant for CMC Laboratories, a technology solutions company that provides analytical and lab-scale plating services, program management, and marketing research for clients focusing on advanced materials and all levels of electronic interconnection.

Thomas (Tom) Beckett has been working in the metal finishing industry for more than 30 years. Beckett has extensive experience

# TECHNICALLY speaking

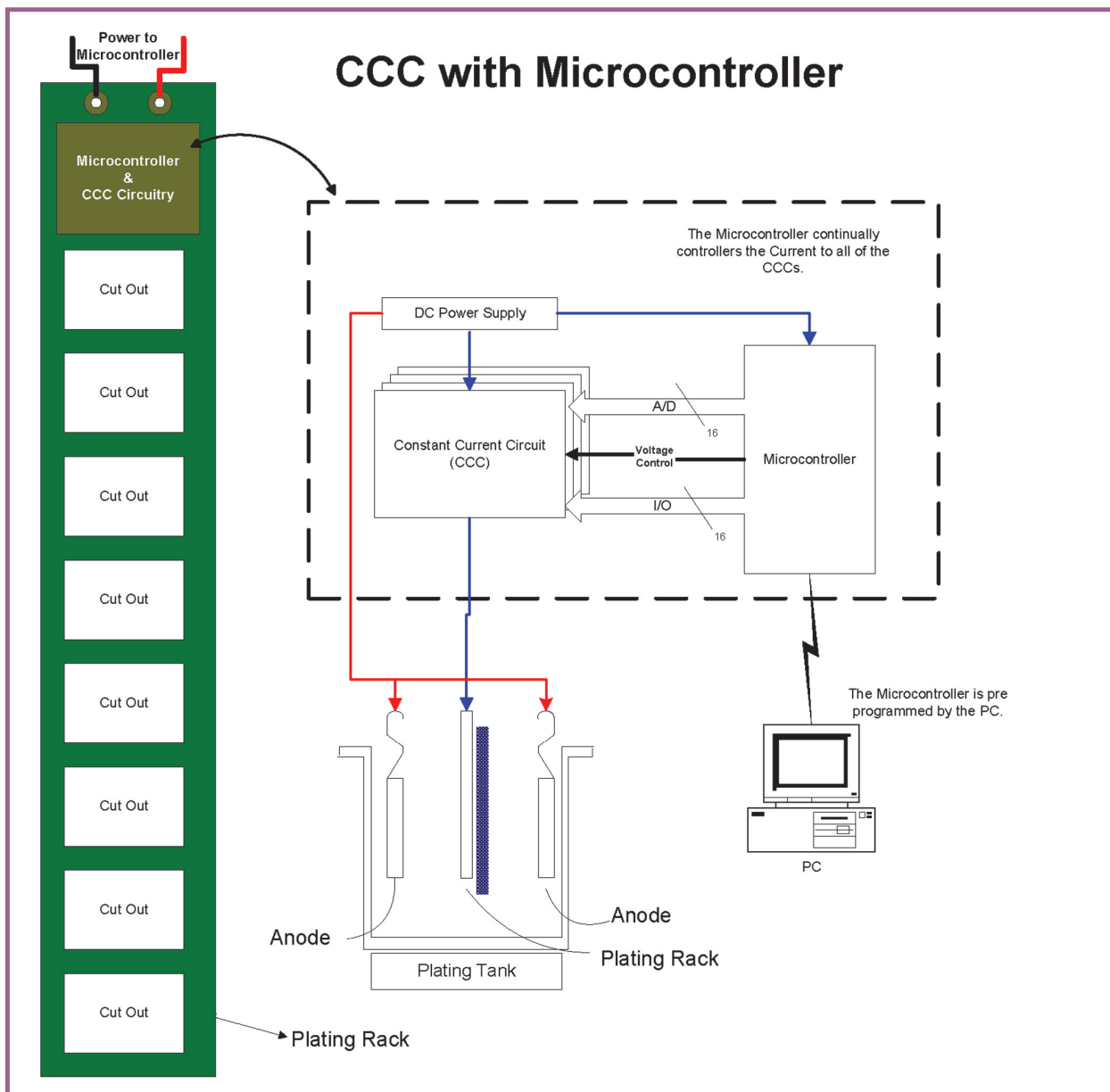


Figure 7. Schematic of the control circuit.

with electrochemical and finishing processes such as cleaning, phosphating, organic finishing, and base metal plating, including nickel-chrome, precious metals, electroless nickels and gold plating. Beckett has expertise in laboratory procedures, wet analysis, and analytical instrumentation. Beckett has also designed and installed plating equipment for PWB's, nickel-gold tab lines and other specialty installations.

Beckett's professional record includes metal finishing engineering at CMC Wireless Components and Nelco, Inc., where he focused on solving existing issues to improve manufacturing processes, productivity and yield. Tom currently provides professional plating engineering assistance through his company, Tom

Beckett Electrochemical Consulting.

Beckett received his BS in Bio-Chemistry from Chicago State University in Chicago, Illinois, with a minor in Physical Science and Mathematics.

**Gabe Carrasco** is a senior test engineer. Drawing from more than 10 years experience in testing ceramic packaging, Carrasco has the knowledge, experience, and judgment needed to apply measurements in the most effective manner. He held key technical and management positions while serving with Carborundum and CMC Wireless Components, starting with senior Q/A technician and advancing to test engineer, manufacturing manager, and



# TECHNICALLYspeaking

*then vice president of operations. For CMC Laboratories, Carrasco serves as the Sr. Test Engineer overseeing the Environmental, Thermal and RF/Electrical testing.*

**Dr. J. Harris** has played a leadership role in the advanced ceramic materials and electronic packaging industry over the past 20 years. Dr. Harris is currently the President of CMC Laboratories, Inc., a materials analysis and consulting firm that focuses on advanced materials used in electronic applications. CMC provides a range of technology services, including materials related consulting, materials characterization, analytical services, prototype fabrication, and technology licensing. Dr. Harris received his doctorate in Solid State Physics from Brown University (Providence, RI) in 1983. He is the author of more than 50 publications and book chapters and has 20 US Patents.

**Erich Rubel** is director, analytical services. He has more than 20 years of experience working in quality, R&D, and failure analysis laboratories serving both the electronics and aerospace industry. His educational and technical focus spans the fields of chemistry, metallurgy, and materials science. Rubel gained extensive familiarity with advanced materials and processes while working at Honeywell, Inc. and later at CMC Wireless Components. He currently manages the SEM and Metallurgical Laboratories at CMC Laboratories.

## REFERENCES

1. Submitted to U.S. Patent Office
2. Semiconductor International, Oct. 1, 2007